AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 5, line 23, with the following rewritten paragraph:

According to a 1st aspect of the present invention, there is provided a video signal processor comprising: a memory that utilizes a first clock signal for writing a video data signal and a second clock signal for reading a video data signal; a delay unit, including plural delay elements, for delaying the second clock signal; a selector for selecting a clock that is most synchronized with a reference signal inputted from outside, from among clocks that have been delayed using the respective delay elements of the delay unit, and ~~outputs~~outputting phase information of the selected clock; an interpolation factor output unit for converting the phase information into an interpolation factor, and outputting the interpolation factor; and an interpolator for interpolating the video data signal read from the memory in accordance with the second clock signal using the interpolation factor. Therefore, it is possible to prevent one period of the clock from becoming a length that is not within a specified range in selecting a clock so as to be in phase with the reference signal. Further, it is possible to avoid an arithmetic error or malfunction in the video signal processor or in a later stage apparatus, which would otherwise arise due to shortening of the period of the clock.

Please replace the paragraph at page 6, line 18, with the following rewritten paragraph:

According to a 2nd aspect of the present invention, there is provided a video signal processor comprising: a memory that utilizes a first clock signal for writing a video data signal and a second clock signal for reading a video data signal; a delay unit, including plural delay elements that can vary respective delay ~~elements~~values, for delaying the second clock signal by one period of the second clock signal; a phase comparator for comparing phases between a clock that is obtained by delaying a focus clock in the second clock signal by one clock using the delay unit, and a clock that is one clock later than the focus clock; a controller for controlling respective delay values of the delay elements of the delay unit on the basis of a phase difference detected by the phase comparator; a selector for selecting a clock that is most synchronized with a reference signal inputted from outside, from among clocks that have been delayed by the respective delay elements of the delay unit, and outputting phase information of the selected clock; an interpolation factor output unit for

converting the phase information into an interpolation factor, and outputting the interpolation factor; and an interpolator for interpolating the video data signal read from the memory in accordance with the second clock signal using the interpolation factor. Therefore, even when there are temperature variations or abrupt changes in the reference signal, it is possible to keep constant the frequencies of the clocks that are outputted from the respective delay elements. In addition, it is possible to prevent one period of the clock from becoming a length that is not within a specified range in selecting a clock so as to be in phase with the reference signal. Further, it is possible to avoid an arithmetic error or malfunction in the video signal processor or in a later stage apparatus, which would otherwise arise due to shortening of the period of the clock.

Please replace the paragraph at page 8, line 19, with the following rewritten paragraph:

According to a 4th aspect of the present invention, there is provided a video signal processor comprising: a memory that utilizes a first clock signal for writing or reading a video data signal; a delay unit, including plural delay elements that can vary respective delay values, for delaying the first clock signal by one period of the first clock signal; a phase comparator for comparing phases between a clock that is obtained by delaying a focus clock in the first clock signal by one clock using the delay unit, and a clock that is one clock later than the focus clock; a controller for controlling the respective delay values of the delay elements of the delay unit on the basis of a phase difference detected by the phase comparator; a selector for selecting a clock that is most synchronized with a reference signal inputted from outside, from among clocks that have been delayed by the delay elements of the delay unit, and outputting phase information of the selected clock; an interpolation factor output unit for converting the phase information into an interpolation factor, and outputting the interpolation factor; and an interpolator for ~~interpolation~~interpolating the video data signal read from the memory in accordance with the first clock signal using the interpolation factor. Therefore, even when there are temperature changes or abrupt changes in the reference signal, it is possible to keep constant the frequencies of the clocks that are outputted from the delay elements. Further, it is possible to prevent one period of the clock from becoming a length that is not within a specified

range in selecting a clock so as to be in phase with the reference signal. Further, it is possible to avoid an arithmetic error or malfunction in the video signal processor or in a later stage apparatus, which would otherwise arise due to shortening of the period of the clock.

Please replace the paragraph at page 14, line 8, with the following rewritten paragraph:

As shown in figure 2, the interpolation circuit 111 includes a delay circuit 201 for delaying the output video data signal S110 read from the memory 110 in accordance with the second clock signal S102, by a time corresponding to one period of the second clock signal S102, a subtraction circuit 202 for subtracting a delay circuit output signal S201 from the output video data signal ~~S202~~S110, a multiplication circuit 203 for multiplying a subtraction circuit output signal S202 by the interpolation factor S109, and an addition circuit 204 for adding the delay circuit output signal S201 and a multiplication circuit output signal S203.

Please replace the paragraph at page 22, line 10, with the following rewritten paragraph:

The video signal processor according to the second embodiment does not ~~interpolates~~ interpolate the video data signal S100 using the second clock signal S102 but interpolates the output video data signal S110 using the first clock signal that is used to write the video data signal S100 in the memory 110.

Please replace the paragraph at page 26, line 9, with the following rewritten paragraph:

As described above, the video signal processor according to the second embodiment includes the memory 110 ~~that~~which utilizes the first clock signal S101 as a writing clock for the video data signal S100 and a reading clock for the output video data signal S110, the delay elements 104 to 107 each delaying the first clock signal S101 successively by 1/4 clock, the control circuit 113 ~~that~~which controls the respective delay values of the delay elements 104 to 107 on the basis of the result of the comparison by the phase comparator 112, the selector 108 ~~that~~which selects one of the delayed clocks S104 to S107, delayed by the delay elements 104 to 107, ~~which~~that is the most synchronized with the reference signal S103 inputted from outside, and outputs phase information S108 of the

selected delayed clock, the factor control circuit 109 ~~that~~which converts the phase information S108 into the interpolation factor S109, and the interpolation circuit 111 ~~that~~which interpolates the output video data signal S110 read from the memory 110 in accordance with the first clock signal S101, using the interpolation factor S109 and outputs the output video data signal S111. Therefore, in changing the clock so as to be in phase with the reference signal S103, it is possible to prevent one period of the clock from becoming a length that is not within a specified range. Further, an arithmetic error or malfunction in the video signal processor resulting from the reduction of the period of the clock can be avoided.